What is claimed is:

1. A nonvolatile semiconductor memory device comprising:

a channel forming region comprised of a semiconductor;

a charge storing film including a plurality of stacked dielectric films and having a charge storing capability;

two storage portions comprised of regions of the charge storing film overlapping the two ends of the channel forming region;

a single layer dielectric film contacting the channel forming region between the two storage portions;

a control gate electrode contacting the single layer dielectric film; and

a memory gate electrode contacting the two storage portions and having portions contacting the storage portions electrically connected with each other.

2. A nonvolatile semiconductor memory device according to claim 1, wherein the channel forming region comprises:

two outside channel regions facing said memory gate electrode across said storage portions; and

an inside channel region located between the two outside channel regions and facing said control gate

electrode across said single layer dielectric film, and

wherein threshold voltages of the three kinds of channel regions of the two outside channel regions and the inside channel region are controlled independently.

3. A nonvolatile semiconductor memory device according to claim 2, wherein said threshold voltages of said two outside channel regions are equal.

4. A nonvolatile semiconductor memory device according to claim 3, wherein said threshold voltages of the two outside channel regions are lower than the threshold voltage of said inside channel region.

5. A nonvolatile semiconductor memory device according to claim 1, wherein said channel forming region comprises:

two outside channel regions facing said memory gate electrode across said storage portion; and

an inside channel region located between the two outside channel regions and facing said control gate electrode across said single layer dielectric film, and

wherein a length of the inside channel region defined by the distance between the two outside channel regions is a length enabling carriers to move quasi-ballistically in a channel formed at the time of operation.

6. A nonvolatile semiconductor memory device

according to claim 1, wherein said memory gate electrode intersects said control gate electrode in an electrically insulated state and contacts said storage portions at both the outsides of the control gate electrode.

7. A nonvolatile semiconductor memory device according to claim 6, further comprising on said control gate electrode an etching stop layer comprised of a dielectric with an etching rate lower than that of a conductive material forming said memory gate electrode.

8. A nonvolatile semiconductor memory device according to claim 1,

further comprising two impurity regions separated from each other from said storage portion sides across said channel forming region and comprised of a semiconductor having a reverse conductivity type to the channel forming region, and

wherein the two impurity regions are bit lines,

wherein said memory gate electrode is a word line for controlling operations including input and output of charges to or from the storage portions, and

wherein the control gate electrode is a control line for assisting the operations.

9. A nonvolatile semiconductor memory device according to claim 1, wherein

the memory cell comprises:

two impurity regions isolated from each other across said channel forming region from the storage portion sides and comprised of a semiconductor having a conductivity type opposite to the channel forming region;

a control transistor having said control gate electrode as a gate and functioning to make two outside channel regions facing the memory gate electrode across the storage portions the source and the drain; and

two memory transistors connected in series across said control transistor, each having said memory gate electrode as the gate, and each functioning to make the channel region between the control transistor and one of the two impurity regions as a source or a drain, and wherein:

a plurality of such memory cells are arranged in a matrix to form a memory cell array;

each of the two impurity regions is arranged long in one direction of said memory cell array and is shared among a plurality of memory cells; and

the control gate electrode is arranged in the space separating the two impurity regions parallel to the impurity regions and is shared among the plurality of memory cells.

10. A nonvolatile semiconductor memory device according to claim 9, wherein each of said two impurity

regions is isolated from an impurity region of another memory cell adjoining in a direction perpendicular to the longitudinal direction.

11. A nonvolatile semiconductor memory device according to claim 9, wherein each of said two impurity regions is shared among memory cells adjoining in a direction perpendicular to the longidinal direction.

12. A nonvolatile semiconductor memory device according to claim 9, wherein memory cells adjoining in one direction are isolated by a dielectric isolation layer.

13. A nonvolatile semiconductor memory device according to claim 12, wherein said dielectric isolation layer is arranged in stripes parallel to said memory gate electrodes beneath a space between the memory gate electrodes.

14. A nonvolatile semiconductor memory device according to claim 12, wherein said dielectric isolation layer is arranged along said memory gate electrodes beneath a space between the memory gate electrodes and separated on said impurity regions.

15. A nonvolatile semiconductor memory device according to claim 12, wherein

said memory gate electrode has sidewalls at the two sides in the width direction, and

each of the sidewalls is overlapped with an edge of said dielectric isolation layer across said charge storing film in a region adjoining said storage portion.

16. A method for operating a nonvolatile semiconductor memory device comprising a channel forming region comprised of a first conductivity type semiconductor, two impurity regions comprised of a second conductivity type semiconductor and separated from each other across the channel forming region, a charge storing film including a plurality of stacked dielectric films and having a charge storing capability, two storage portions comprised of regions of the charge storing film overlapping with two ends of the channel forming region at the two impurity region sides, a single layer dielectric film contacting the channel forming region between the storage portions, a memory gate electrode contacting the storage portions, and a control gate electrode on the single layer dielectric film,

said operation including a write operation comprising the steps of:

applying a predetermined voltage between the two impurity regions so as to make the impurity region located near the storage portion side to be written the drain and to make the other the source;

applying a specified voltage to each of the memory gate electrode and the control gate electrode to form a channel between the two impurity regions; and

injecting part of the carriers injecting in the channel into the drain side storage portion.

17. A method for operation of a nonvolatile semiconductor memory device according to claim 16, comprising, in the step of forming the channel, controlling the values of voltages applied to said memory gate electrode and said control gate electrode to form a channel having a channel resistance beneath said two storage portions different from a channel resistance beneath said single layer dielectric film between the two impurity regions.

18. A method for operating a nonvolatile semiconductor memory device according to claim 16, comprising, in the step of forming the channel, a step of controlling the values of voltages applied to said memory gate electrode and said control gate electrode to generate a high electric field in a channel region beneath the control gate electrode and in a region of the first conductivity type semiconductor beneath a space between the control gate electrode and the memory gate electrode along the direction of charge injection in the channel.

19. A method for operating a nonvolatile semiconductor memory device comprising a channel forming region comprised of a first conductivity type semiconductor, two impurity regions comprised of a second conductivity type semiconductor and separated from each other across the channel forming region, a charge storing film including a plurality of stacked dielectric films and having a charge storing capability, two storage portions comprised of regions of the charge storing film overlapping with two ends of the channel forming region at the two impurity region sides, a single layer dielectric film contacting the channel forming region between the storage portions, a memory gate electrode contacting the storage portions, and a control gate electrode on the single layer dielectric film,

said operation including a write operation comprising the steps of:

applying a voltage between the memory gate electrode and the impurity region located at the storage portion side where the data is to be written in a direction so as to invert the impurity region;

generating a high energy charges by avalanche breakdown caused in an inversion layer of the impurity region at the time of applying the voltage; and

injecting part of the generated high energy

charge into the storage portion of the side where data is to be written.

20. A method for operating a nonvolatile semiconductor memory device according to claim 19, comprising, in said write operation, changing the potential in said channel forming region beneath said single layer dielectric film according to the potential of the control gate electrode to control the injection position of the high energy charges.

21. A method for operating a nonvolatile semiconductor memory device according to claim 16 including an erasure operation comprising the steps of:

applying a voltage for inversion of the impurity region between the impurity region located at the side of the storage portion retaining the stored data to be erased and said memory gate electrode;

generating high energy charges of a polarity opposite to the charge injected at the time of the write operation due to avalanche breakdown or a band-to-band tunneling caused at an inversion layer of the impurity region at the time of applying the voltage; and

injecting part of the generated high energy charge into the storage portion retaining the stored data.

22. A method for operating a nonvolatile

semiconductor memory device according to claim 19 including an erasure operation comprising the steps of:

applying a predetermined voltage between said two impurity regions so as to make the impurity region at the side of the storage portion retaining the stored data to be erased the drain and to make the other impurity region the source;

applying specified voltages to each of the memory gate electrode and the control gate electrode to form a channel between the two impurity regions; and

injecting part of the carriers having an opposite polarity to the charge injected at the time of the write operation and injecting in the channel into the storage portion retaining the stored data to be erased.

23. A method for operating a nonvolatile semiconductor memory device according to claim 22, comprising, in the step of forming the channel, a step of controlling the values of voltages applied to said memory gate electrode and said control gate electrode to form a channel having a channel resistance beneath said two storage portions different from a channel resistance beneath said single layer dielectric film between the two impurity regions.

24. A method for operating a nonvolatile semiconductor memory device according to claim 16

including a read operation comprising the steps of:

applying a voltage between said two impurity regions so as to make the impurity region at the side of the storage portion retaining the stored data to be read the source and to make the other impurity region the drain;

applying specified voltages to each of said memory gate electrode and said control gate electrode; and

changing the presence or absence of charge or the difference of amount of charge in the storage portion according to the stored data into the amount of current flowing in the channel forming region or the amount of change of voltage of the impurity regions to read the stored data.

25. A method for operating a nonvolatile semiconductor memory device according to claim 19 including a read operation comprising the steps of:

applying a voltage between said two impurity regions so as to make the impurity region at the side of the storage portion retaining the stored data to be read the source and to make the other impurity region the drain;

applying specified voltages to each of said memory gate electrode and said control gate electrode;

and

changing the presence or absence of charge or the difference of amount of charge in the storage portion according to the stored data into the amount of current flowing in the channel forming region or the amount of change of voltage of the impurity region to read the stored data.

26. A method for operating a nonvolatile semiconductor memory device comprising memory cells arranged in a matrix to form a memory cell array, each of said each memory cell comprising a channel forming region comprised of a first conductivity type semiconductor, two impurity regions comprised of a second conductivity type semiconductor and separated from each other across the channel forming region, a charge storing film including a plurality of stacked dielectric films and having a charge storing capability, two storage portions comprised of regions of the charge storing film overlapping with two ends of the channel forming region at the two impurity region sides, a single layer dielectric film contacting the channel forming region between the storage portions, a memory gate electrode contacting the storage portions, and a control gate electrode on the single layer dielectric film; the memory gate electrode being shared among a plurality of cells in the direction of separation

of the impurity regions and comprising a word line; each of the two impurity regions being shared among a plurality of cells in the direction perpendicular to the word line and comprising a bit line; and the control gate electrode being arranged in parallel to the bit line and shared among a plurality of cells in a direction perpendicular to the word line,

said method including a read operation comprising a step of applying a voltage of a direction giving a forward bias to the channel forming region to a nonselected word line in a row not including the memory cell to be read.

27. A method for operating a nonvolatile semiconductor memory device according to claim 26, wherein

said memory cell has two storage portions at the sides of the two impurity regions and,

in said memory cell, a control transistor having a control gate electrode as a gate and functioning to make two outside channel regions facing said memory gate electrode across the two storage portions the source and drain and two memory transistors having said memory gate electrode as a gate and functioning to make the channel region of the control transistor and one of the

two impurity regions the source or drain connected in series across the control transistor.

28. A method for operating a nonvolatile semiconductor memory device according to claim 26 comprising, in the step of applying a voltage of a direction giving a forward bias, a step of applying a minus side voltage with respect to the source voltage to the nonselected word line when said channel forming region is a p-type semiconductor.

29. A method for operating a nonvolatile semiconductor memory device according to claim 26, wherein said voltage of a direction giving a forward bias is a value within a voltage range where memory cells connected to a nonselected word line and arranged in the same column as the memory cell to be read are not read erroneously.

30. A method for operating a nonvolatile semiconductor memory device according to claim 26, wherein an absolute value of said voltage in a direction giving a forward bias is smaller than 1V.

31. A method for operating a nonvolatile semiconductor memory device comprising a plurality of memory cells arranged in a matrix to form a memory cell array, each of said each memory cell comprising a channel forming region comprised of a first conductivity type

32. A method for operating a nonvolatile semiconductor memory device according to claim 31 wherein said write or erasure operation comprises the steps of:

applying a predetermined voltage between said two impurity regions so as to make the impurity region at the side of the storage portion where memory data is to be written the drain and to make the other impurity region the source;

applying specified voltages to said memory gate electrode and said control gate electrode to form a channel between the two impurity regions; and

injecting part of the carriers injecting in the channel into the drain side storage portion.

33. A method for operating a nonvolatile semiconductor memory device according to claim 32, comprising, in said step of forming a channel, a step of controlling the values of voltages applied to said memory gate electrode and said control gate electrode to form a channel having a channel resistance beneath said two storage portions different from a channel resistance beneath said single layer dielectric film between the two impurity regions.

34. A method for operating a nonvolatile semiconductor memory device according to claim 31, comprising the steps of:

semiconductor, two impurity regions comprised of a second conductivity type semiconductor and separated from each other across the channel forming region, a charge storing film including a plurality of stacked dielectric films and having a charge storing capability, two storage portions comprised of regions of the charge storing film overlapping with two ends of the channel forming region at the two impurity region sides, a single layer dielectric film contacting the channel forming region between the storage portions, a memory gate electrode contacting the storage portions, and a control gate electrode on the single layer dielectric film; the memory gate electrodes in the same row being connected by a word line; each of the two impurity regions being arranged long in the column direction and shared between memory cells adjoining in the row direction; and the control gate electrode being arranged long in the column direction and shared between memory cells in the same column,

said method comprising the steps of:

driving the control gate electrodes to divide the memory cell array electrically; and

driving the impurity regions and the word lines to write, read, or erase data in parallel a plurality of cells in the divided memory cell array.

applying at every certain number of control gate electrodes an off voltage for shifting a memory cell to an inactive state where the channel is unable to be turned on;

writing, reading, or erasing in parallel memory cells in the active state between memory cells placed in the inactive state due to the division; and

repeating the step of dividing the memory cell array and the step of writing, reading, or erasing the memory cells in the active state while shifting the control gate electrodes to which the off voltage is applied in one direction.

35. A method for operating a nonvolatile semiconductor memory device comprising a plurality of memory cells arranged in a matrix to form a memory cell array, each of said each memory cell comprising a channel forming region comprised of a first conductivity type semiconductor, two impurity regions comprised of a second conductivity type semiconductor and separated from each other across the channel forming region, a charge storing film including a plurality of stacked dielectric films and having a charge storing capability, two storage portions comprised of regions of the charge storing film overlapping with two ends of the channel forming region at the two impurity region sides, a single layer

dielectric film contacting the channel forming region between the storage portions, a memory gate electrode contacting the storage portions, and a control gate electrode on the single layer dielectric film; the memory gate electrodes in the same row being connected by a word line; each of the two impurity regions being arranged long in the column direction and shared between memory cells adjoining in the row direction; and the control gate electrode being arranged long in the column direction and shared between memory cells in the same column,

the method including a write operation comprising the steps of:

alternately applying a write drain voltage and a reference voltage to the impurity regions in the memory cell array;

applying an ON voltage for shifting a channel from an OFF state to a possible ON state to the control gate electrode in combination according to the data to be written;

selecting a storage portion located between the control gate electrode applied with the ON voltage and the impurity region applied with the write drain voltage;

applying a specified voltage to a word line of a selected row in which the data is to be written to turn

the channel on beneath the selected storage portion and injecting part of the carriers injecting in the channel in the selected storage portion;

reapplying the write drain voltage and reference voltage to the impurity regions in the memory cell array while switching the locations of application;

reapplying the ON voltage to the control gate electrode in combination according to the data to be written;

selecting the remaining storage portion different from above storage portion; and

reapplying the voltage to the word line and turn the channel on beneath the selected storage portion and injecting part of the carriers injecting in the channel in the selected storage portion.

36. A method for operating a nonvolatile semiconductor memory device according to claim 35, comprising the steps of:

fixing the potential of the impurity regions and in that state successively selecting the word line to which the memory cell to be written with data is connected and repeating the selection of the storage portion and the injection of carrier into the selected storage portion while changing the application of the ON voltage to the control gate electrode according to the

data to be written for each selected word line for all word lines in the memory cell array;

reapplying the write drain voltage and reference voltage to the impurity regions in the memory cell array while switching the locations of application; and

fixing the potential of the impurity regions and in that state successively selecting the word line to which the memory cell to be written with data is connected and repeating the selection of the storage portion and the injection of carrier into the selected storage portion while changing the application of the ON voltage to the control gate electrode according to the data to be written for each selected word line for all word lines in the memory cell array.

37. A method for operating a nonvolatile semiconductor memory device comprising a plurality of memory cells arranged in a matrix to form a memory cell array, each of said each memory cell comprising a channel forming region comprised of a first conductivity type semiconductor, two impurity regions comprised of a second conductivity type semiconductor and separated from each other across the channel forming region, a charge storing film including a plurality of stacked dielectric films and having a charge storing capability, two storage

portions comprised of regions of the charge storing film overlapping with two ends of the channel forming region at the two impurity region sides, a single layer dielectric film contacting the channel forming region between the storage portions, a memory gate electrode contacting the storage portions, and a control gate electrode on the single layer dielectric film; the memory gate electrodes in the same row being connected by a word line; each of the two impurity regions being arranged long in the column direction and shared between memory cells adjoining in the row direction; and the control gate electrode being arranged long in the column direction and shared between memory cells in the same column,

said method having a read operation comprising the steps of:

a first reading step of reading one storage portion in the odd-numbered memory cells included in same row of the memory cell array;

a second reading step of reading the other storage portion of the odd-numbered memory cells included in the same row;

a third reading step of reading one storage portion of even-numbered memory cells included in the same row; and

a fourth reading step of reading the other storage portion of the even-numbered memory cells included in the same row.

38. A method for operating a nonvolatile semiconductor memory device according to claim 37, wherein said read operation comprises the steps of:

resetting to apply a reference voltage to all of the impurity regions and apply an OFF voltage to all of the control gate electrodes;

selecting the odd-numbered memory cells or the even-numbered memory cells by alternately applying to the control gate electrodes in the memory cell array an ON voltage for shifting a channel from an OFF state to a possible ON state and an OFF voltage for holding the channel in the OFF state;

changing the memory cells selected by switching the application of the ON voltage and the OFF voltage;

alternatively applying to the impurity regions in the memory cell array the reference voltage and the read drain voltage so as to select a pair of the storage portions on the two sides of an impurity region to which the reference voltage is applied; and

changing the pair of storage portions selected by switching the application of the reference voltage and the read drain voltage.

39. A method for operating a nonvolatile semiconductor memory device according to claim 38, wherein a read operation on a plurality of memory cells in the same row comprises the steps of:

resetting;

selecting a pair of storage portions;

performing a first reading operation by selecting a memory cell;

performing a second reading operation by changing the memory cell selected;

resetting;

performing a third reading operation by selecting a memory cell; and

performing a fourth reading operation by changing the memory cell selected.

40. A method for operating a nonvolatile semiconductor memory device according to claim 37, comprising the steps of:

performing one of said first to fourth reading steps repeatedly on all of the word lines in the memory cell array while fixing the voltage application conditions of the impurity regions and the control gate electrodes;

changing the voltage application conditions of the impurity regions and the control gate electrodes to

enable selection of any of the remaining steps among the first to fourth reading steps; and

repeatedly performing the reading steps under constant voltage application conditions for all rows in the memory cell array and the step of changing the voltage application conditions until all of the storage portions in the memory cell array finish being read.

41. A method for producing a nonvolatile semiconductor memory device including a memory cell comprising a channel forming region comprised of a first conductivity type semiconductor, two impurity regions comprised of a second conductivity type semiconductor and separated from each other across the channel forming region, a charge storing film including a plurality of stacked dielectric films and having a charge storing capability, two storage portions comprised of regions of the charge storing film overlapping the two ends of the channel forming region at the two impurity region sides, a single layer dielectric film contacting the channel forming region between the storage portions, a memory gate electrode on the storage portions, and a control gate electrode on the single layer dielectric film,

said method comprising the steps of:

forming on the first conductivity type semiconductor a pattern of the single layer dielectric

film and the control gate electrode on the dielectric film;

forming the charge storing film covering the surface of the pattern and the surface of the first conductivity type semiconductor;

forming sidewalls comprised of a conductive material facing the side faces of the pattern across the charge storing film on the portion of the charge storing film forming the storage portion;

doping a second conductivity type impurity into the first conductivity type semiconductor outside the sidewalls using the sidewalls and the pattern as masks to form the two impurity regions having a second conductivity type; and

forming a conductive film for forming the memory gate electrode together with the sidewalls and processing the conductive film to form the memory gate electrode.

42. A method for producing a nonvolatile semiconductor memory device according to claim 41, comprising the steps of:

doping an impurity for defining the threshold voltage of a part of said channel forming region beneath said control gate electrode into an entire surface region of said first conductivity type semiconductor;

forming the pattern; and

adding the impurity to a part of the channel forming region around the pattern to adjust the threshold voltage thereof.